Electronic Version
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Claims

[c1] An integrated circuit device comprising:
a dynamic random access memory (DRAM) cell having a storage capacitor formed within a deep trench in a substrate and a gate conductor overlying said storage capacitor within said deep trench;
isolation regions on either side of the DRAM cell, the isolation regions extending below the gate conductor; and
a liner comprising a nitride compound adjacent the isolation regions and extending at least between each of the isolation regions and the gate conductor.

[c2] The integrated circuit device of claim 1 wherein the liner comprises a silicon-oxy-nitride compound.

[c3] The integrated circuit device of claim 1 wherein the liner extends alongside and below the isolation regions.

[c4] The integrated circuit device of claim 1 wherein a region adjacent the gate conductor contains a dopant, and further including an oxide layer between the gate conductor and the dopant-containing region, and extending between the isolation regions, wherein the oxide layer and

isolation regions define corner regions of the gate conductor and dopant-containing region, and wherein the liner reduces dopant depletion in the corner regions during subsequent thermal processing of the DRAM cell.

[c5] The integrated circuit device of claim 4 wherein the dopant-containing region adjacent the gate conductor comprises a channel.

[c6] The integrated circuit device of claim 4 wherein the dopant comprises boron.

[c7] The integrated circuit device of claim 1 further including a planar support device adjacent the DRAM cell, the planar support device including a thermally produced oxidation layer.

[c8] The integrated circuit device of claim 1 wherein the storage capacitor of the DRAM cell extends below the isolation regions and liner.

[c9] The integrated circuit device of claim 1 wherein a vertical metal oxide semiconductor field effect transistor (MOSFET) comprising the gate conductor and a boron-doped channel overlies the storage capacitor.

[c10] An integrated circuit device comprising:
a dynamic random access memory (DRAM) cell having a

storage capacitor formed within a deep trench in a silicon substrate and a gate conductor overlying said storage capacitor within said deep trench, a region adjacent the gate conductor containing a boron dopant;
isolation regions on either side of the DRAM cell, the isolation regions extending below the gate conductor;
a liner comprising a silicon-oxy-nitride compound adjacent the isolation regions and extending at least between each of the isolation regions and the gate conductor; and
an oxide layer between the gate conductor and the boron dopant-containing region, and extending between the isolation regions, wherein the oxide layer and isolation regions define corner regions of the gate conductor and boron dopant-containing region, and wherein the liner reduces boron depletion in the corner regions during subsequent thermal processing of the DRAM cell.

[c11] The integrated circuit device of claim 10 wherein the liner extends alongside and below the isolation regions.

[c12] The integrated circuit device of claim 10 wherein the boron dopant-containing region adjacent the gate conductor comprises a channel, and wherein a vertical metal oxide semiconductor field effect transistor (MOSFET) comprising the gate conductor and the boron-doped channel overlies the storage capacitor.

[c13] The integrated circuit device of claim 10 further including a planar support device adjacent the DRAM cell, the planar support device including a thermally produced oxidation layer.

[c14] The integrated circuit device of claim 10 wherein the storage capacitor of the DRAM cell extends below the isolation regions and liner.

[c15] A method of fabricating an integrated circuit device comprising:
providing a substrate;
etching a trench in the substrate;
forming in the trench a dynamic random access memory (DRAM) cell having a storage capacitor at a lower end of the trench and a gate conductor overlying said storage capacitor within said trench;
doping regions in the substrate adjacent the gate conductor;
forming trenches adjacent the DRAM cell, the trenches extending below the gate conductor;
forming an isolation liner comprising a nitride compound in the trenches on either side of the DRAM cell, adjacent the gate conductor;
forming isolation regions in the trenches on either side of the DRAM cell; and
thereafter subjecting the DRAM cell, including the

dopant-containing region adjacent the gate conductor, to elevated temperatures by thermal processing, wherein the nitride-containing isolation liner reduces segregation of the dopant in the region adjacent to the gate conductor as a result of the thermal processing, as compared to an essentially nitrogen-free oxide-containing isolation liner.

[c16] The method of claim 15 wherein the dopant is boron.

[c17] The method of claim 15 wherein the liner comprises a silicon-oxy-nitride compound.

[c18] The method of claim 15 wherein the liner is formed on walls of the trenches on either side of the DRAM cell, such that the liner extends alongside and below the isolation regions.

[c19] The method of claim 15 further including forming an oxide layer between the gate conductor and the dopant-containing region, and extending between the isolation regions, wherein the oxide layer and isolation regions define corner regions of the gate conductor and dopant-containing region, and wherein the liner reduces dopant depletion in the corner regions during subsequent thermal processing.

[c20] The method of claim 15 wherein the storage capacitor of

the DRAM cell extends below the isolation regions and liner.

[c21] The method of claim 15 wherein the thermal processing includes forming a support device on the substrate adjacent the isolation regions.

[c22] The method of claim 15 wherein the regions in the substrate adjacent the gate conductor comprise channels of a vertical metal oxide semiconductor field effect transistor (MOSFET).

[c23] A method of fabricating an integrated circuit device comprising:
providing a silicon substrate;
etching a trench in the substrate;
forming in the trench a dynamic random access memory (DRAM) cell having a storage capacitor at a lower end of the trench, a gate conductor overlying said storage capacitor within said trench, and an oxide layer between the gate conductor and the silicon substrate adjacent the gate conductor;
doping regions in the silicon substrate adjacent the gate conductor with boron;
forming trenches adjacent the DRAM cell, the trenches extending below the gate conductor;
forming an isolation liner comprising a silicon-

oxy-nitride compound in the trenches on either side of the DRAM cell, adjacent the gate conductor;
forming isolation regions in the trenches on either side of the DRAM cell, wherein the oxide layer and isolation regions define corner regions of the gate conductor and boron dopant-containing region; and
thereafter subjecting the DRAM cell, including the boron dopant-containing region adjacent the gate conductor, to elevated temperatures by thermal processing,
wherein the nitride-containing isolation liner reduces segregation of the boron dopant in the corner region adjacent to the gate conductor as a result of the thermal processing, as compared to an essentially nitrogen-free oxide-containing isolation liner.

[c24] The method of claim 23 wherein the liner is formed on walls of the trenches on either side of the DRAM cell, such that the liner extends alongside and below the isolation regions.

[c25] The method of claim 23 wherein the storage capacitor of the DRAM cell extends below the isolation regions and liner.

[c26] The method of claim 23 wherein the thermal processing includes forming a support device on the substrate adjacent the isolation regions.

[c27] The method of claim 23 wherein the regions in the substrate adjacent the gate conductor comprise channels of a vertical metal oxide semiconductor field effect transistor (MOSFET).

[c28] An integrated circuit device comprising:
a silicon substrate having active regions;
a DRAM cell formed within a deep trench between the active regions in the substrate, the DRAM cell having a polysilicon gate conductor; and
an oxidized and nitrided sidewall layer extending continuously along the silicon substrate active regions and the polysilicon gate conductor.

[c29] The integrated circuit device of claim 28 wherein the DRAM cell comprises a vertical MOSFET having the gate conductor and further including a gate oxide layer between the gate conductor and at least one of the active regions in the substrate, and further including a pair of oxidized and nitrided sidewall layers as liners for isolation regions on either side of the DRAM cell and active regions in the substrate.

[c30] A method of fabricating an integrated circuit device comprising:
providing a silicon substrate having active regions;

forming a DRAM cell within a deep trench between the active regions in the substrate, the DRAM cell having a polysilicon gate conductor; and

forming an oxidized and nitrided sidewall layer extending continuously along the silicon substrate active regions and the polysilicon gate conductor.

[c31] The method of claim 30 wherein forming the DRAM cell comprises forming a vertical MOSFET having the gate conductor and a gate oxide layer between the gate conductor and at least one of the active regions in the substrate, and further including forming a pair of oxidized and nitrided sidewall layers as liners for isolation regions on either side of the DRAM cell and active regions in the substrate.